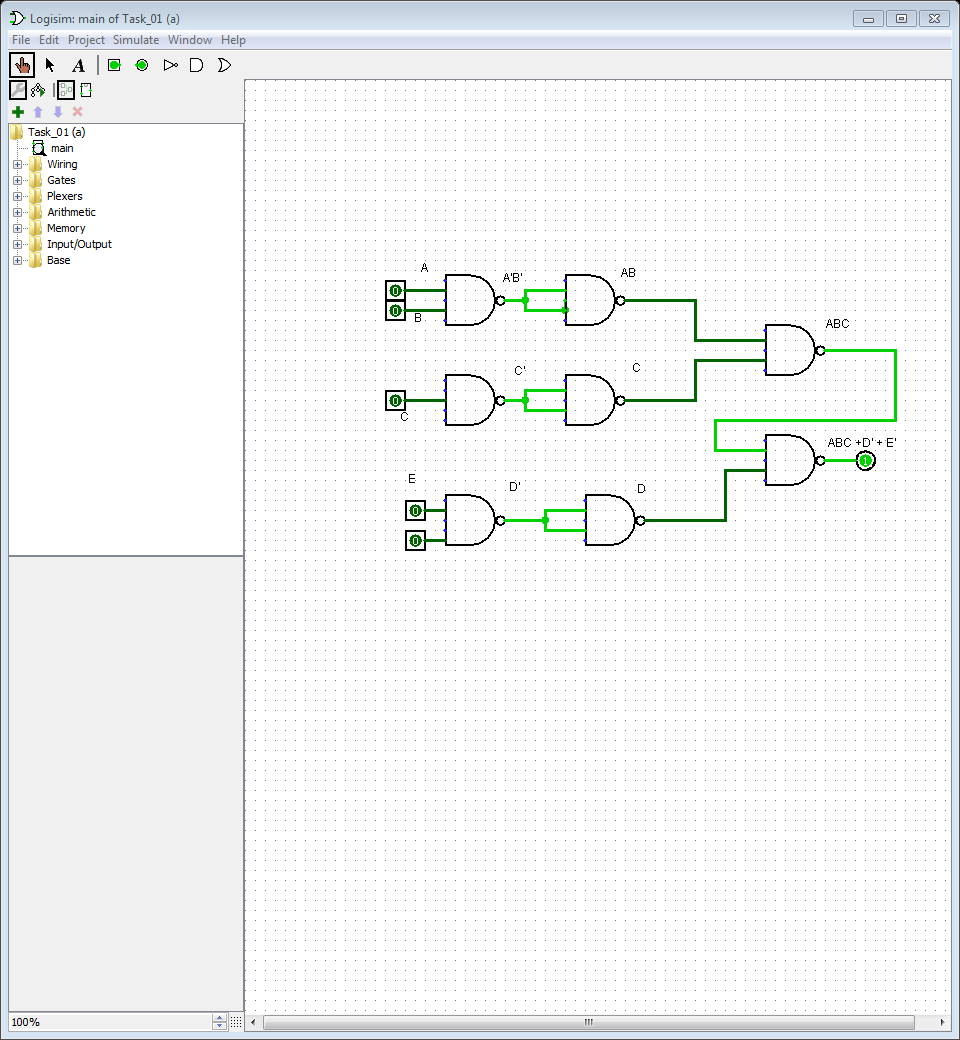
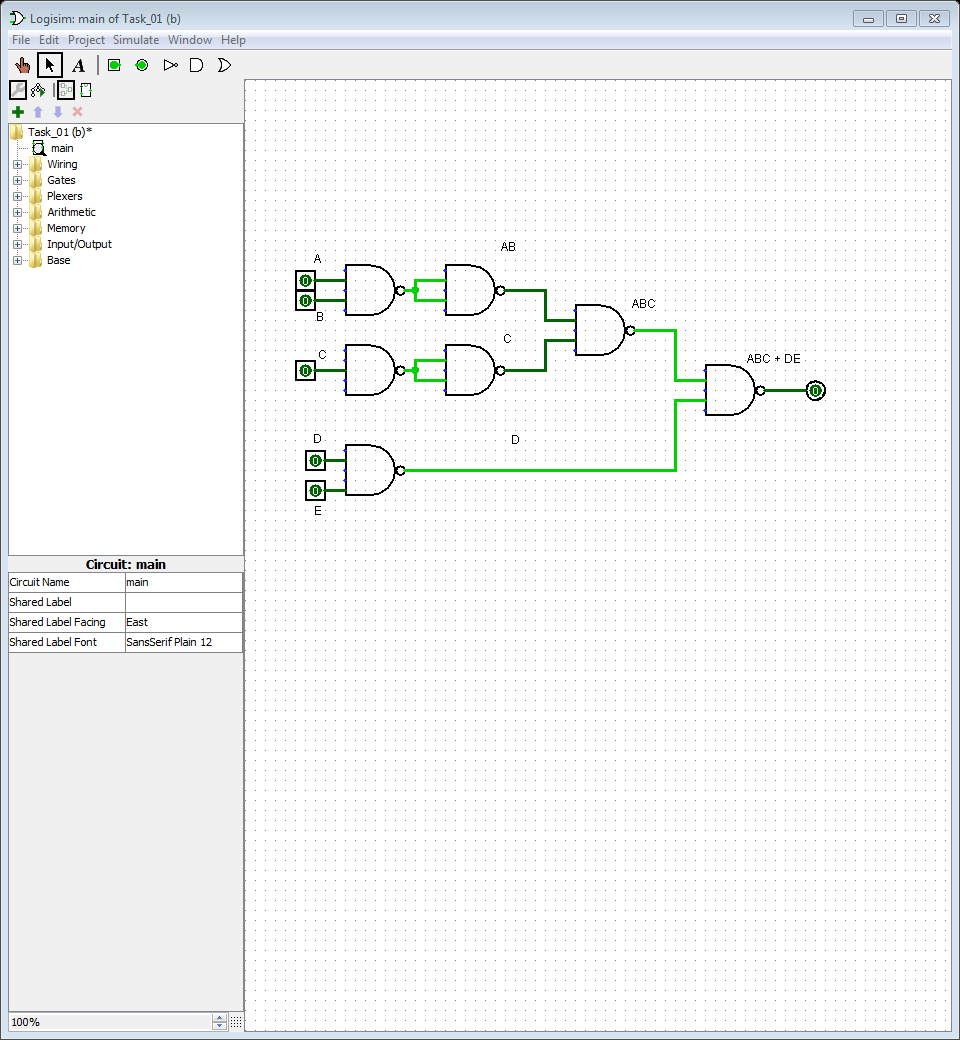
**Question: 01 Design circuit diagram in Logic Works given expressions by using NAND gates**

**only**

1. **ABC + D' + E'**

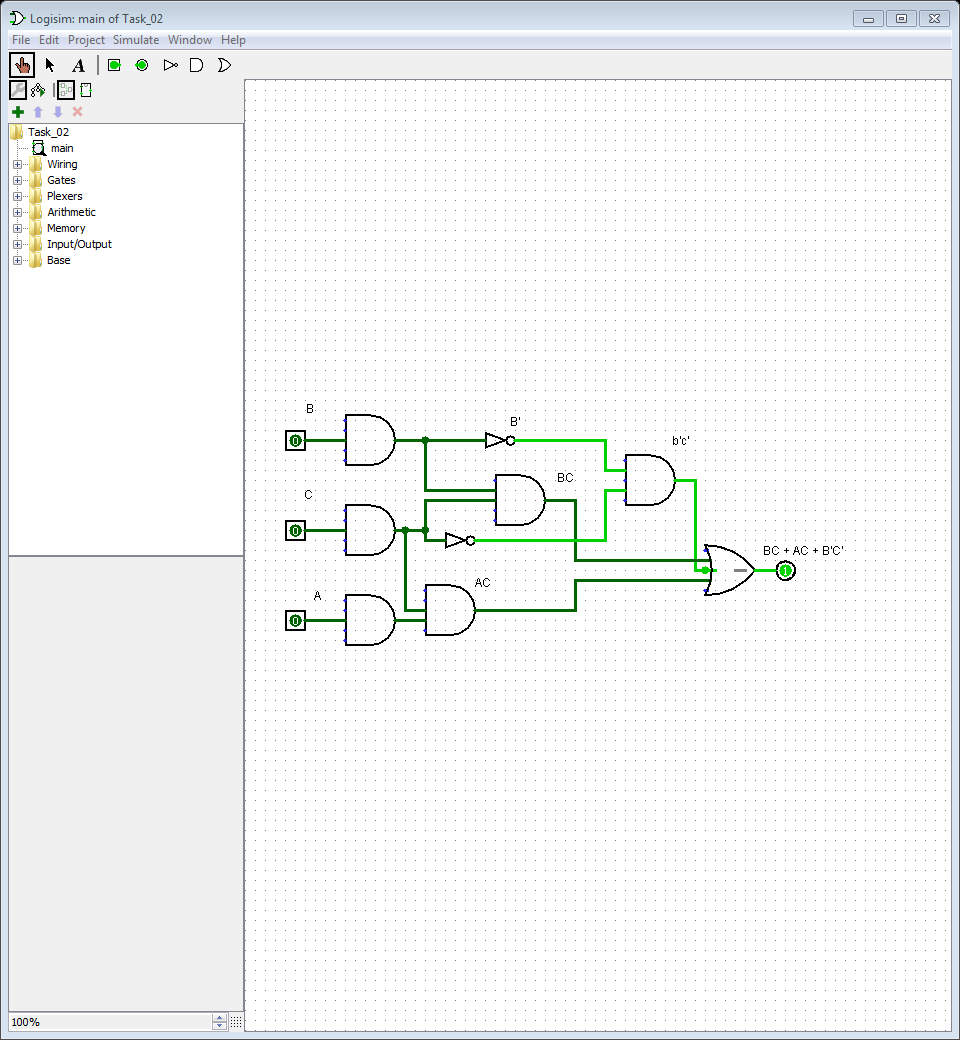
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1. **ABC + DE**



**Question: 02**

**simplify the following Boolean expression: and design circuit in Logisim/Logic Works.**

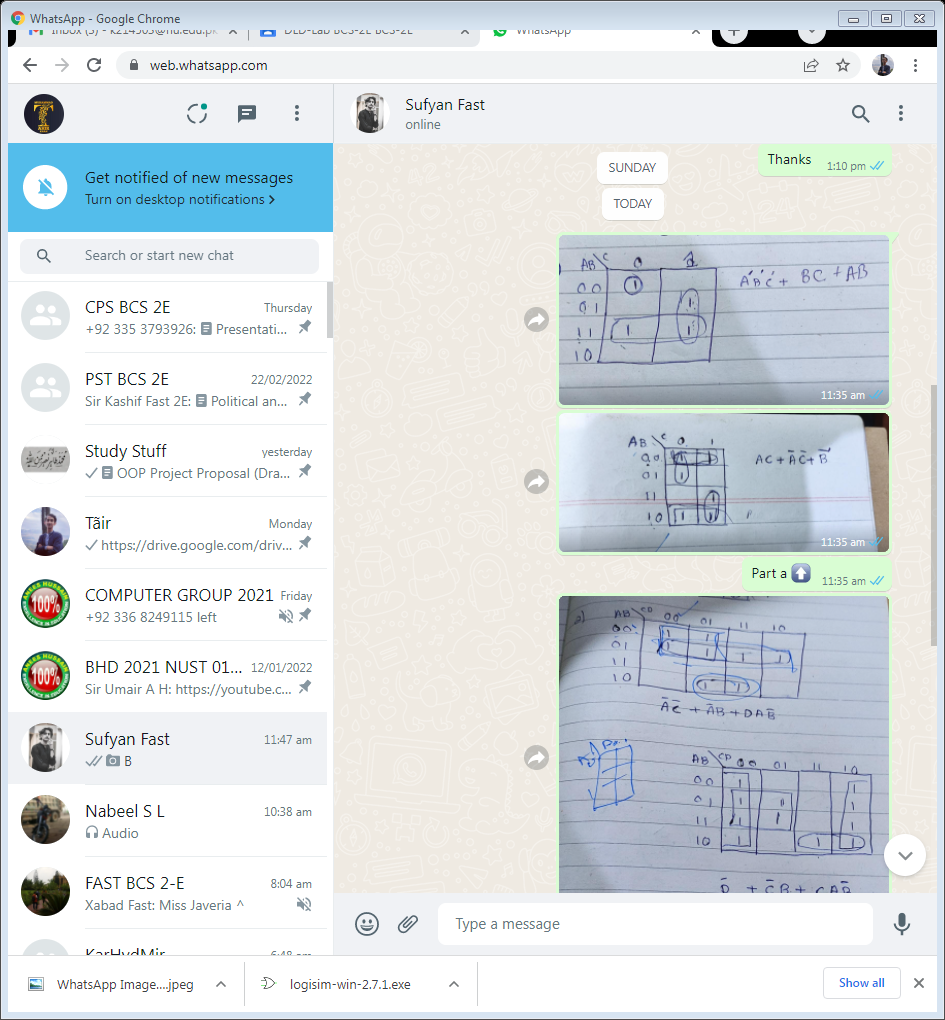
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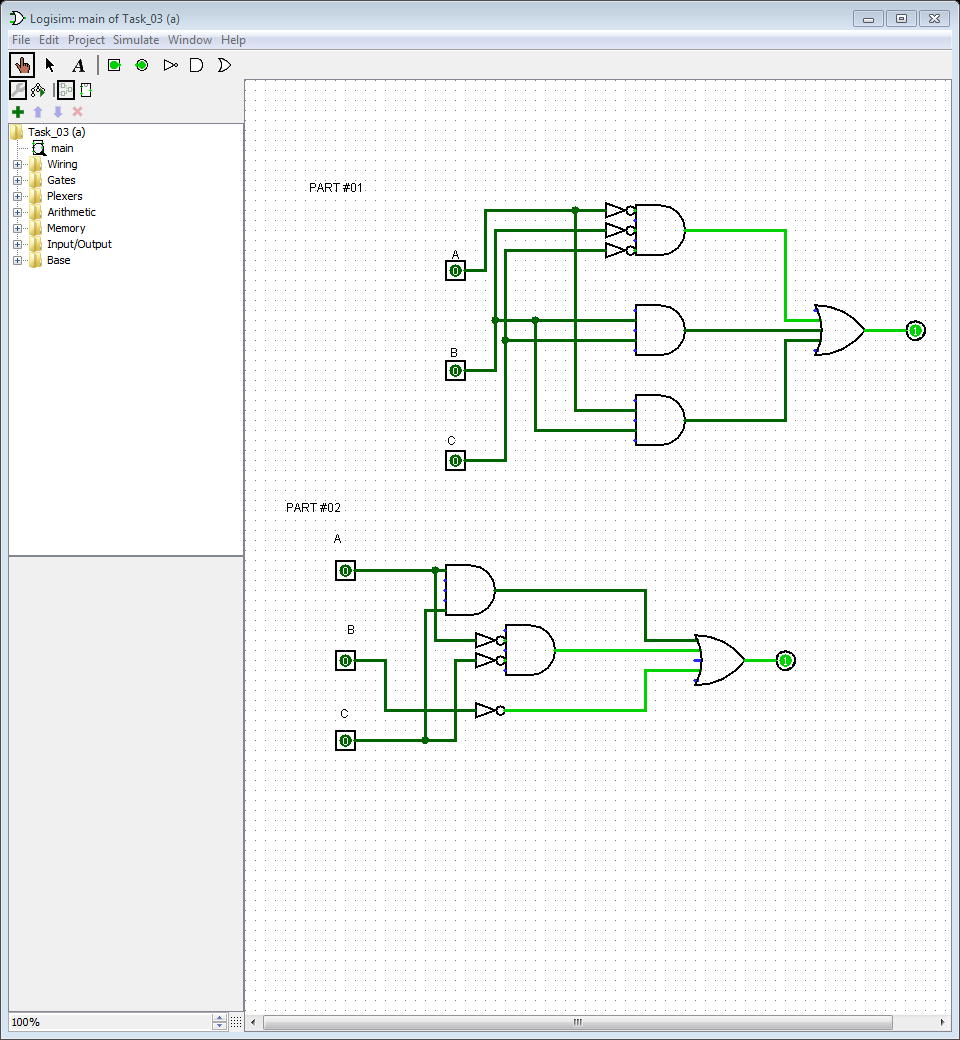
**Question: 03**

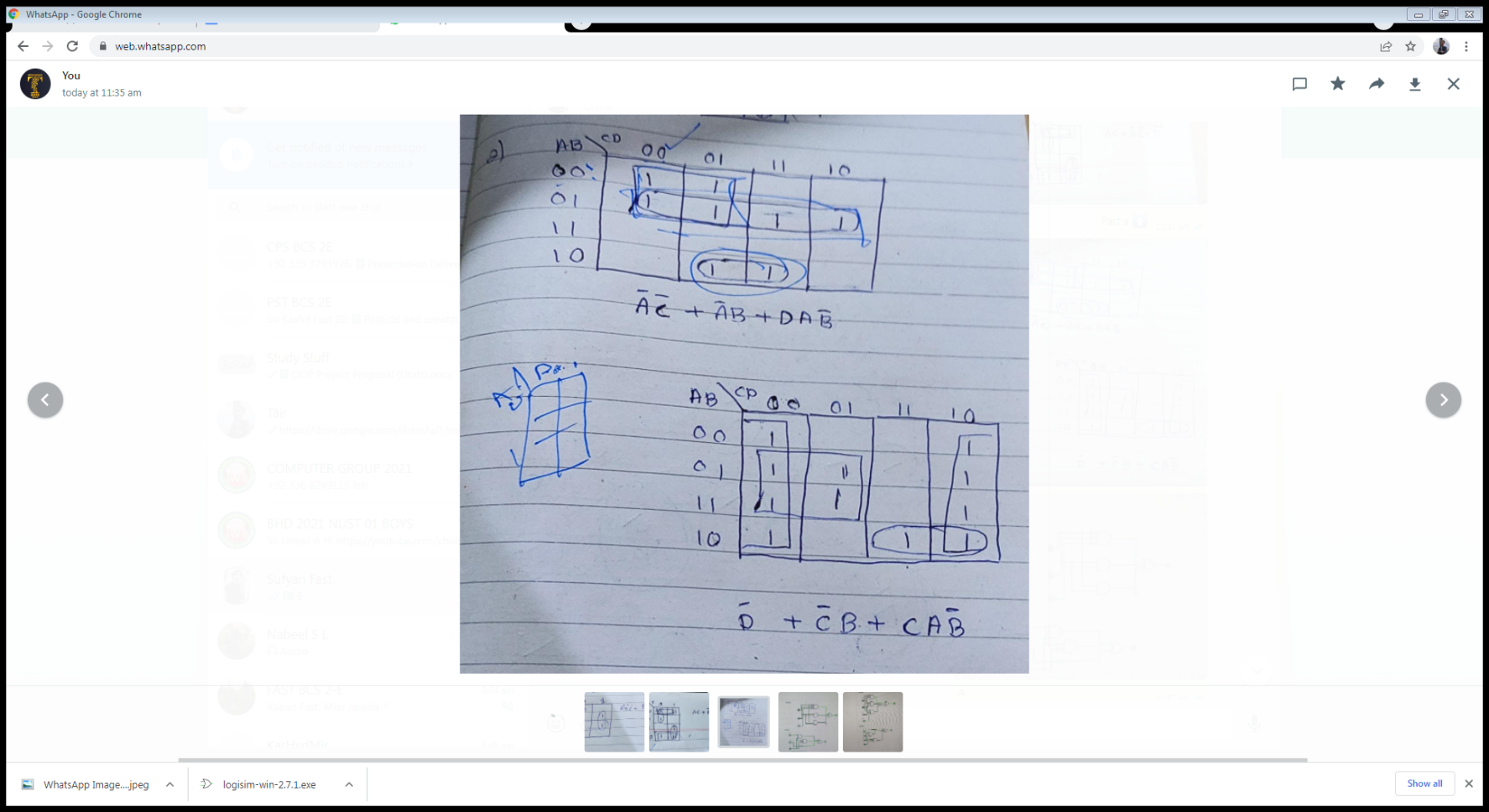
**a. Group the 1s in each of the Karnaugh maps in Figures**

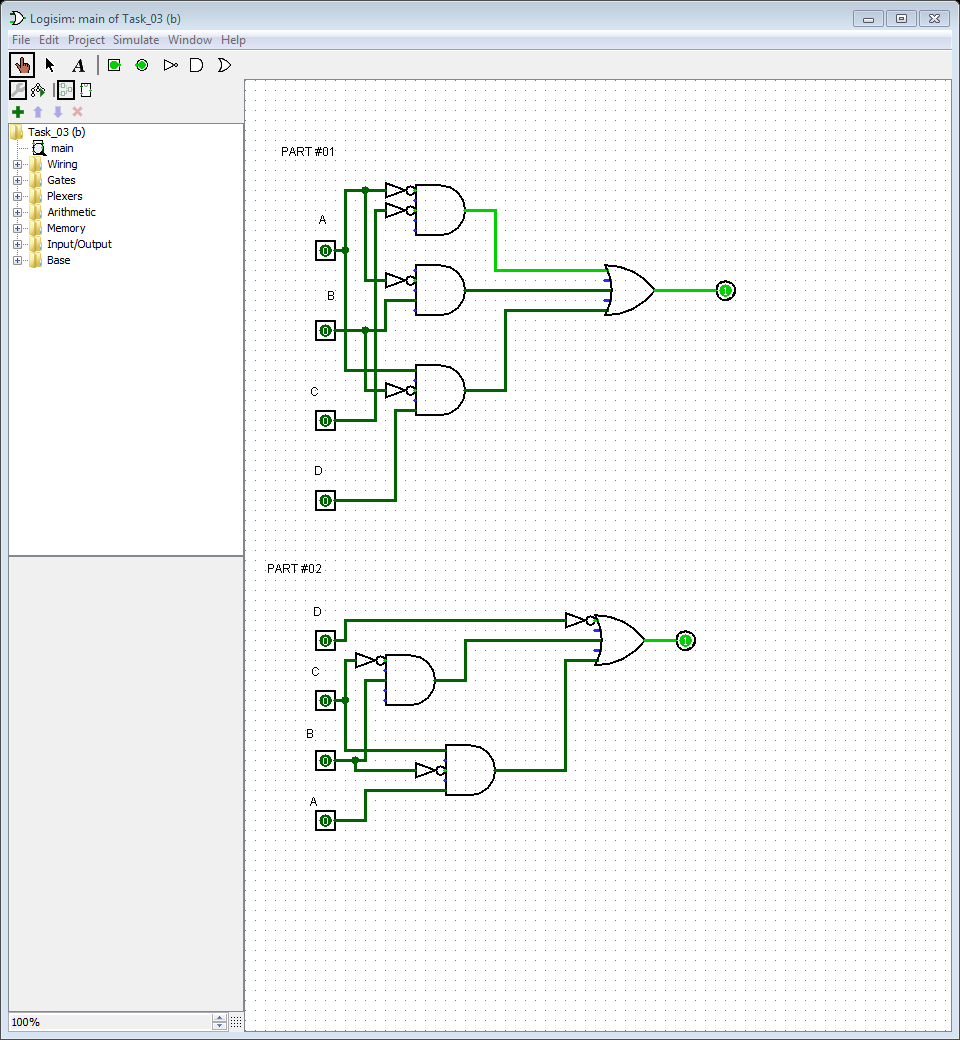
**b. Determine the product terms for each of the Karnaugh maps in Figures and write the resulting minimum SOP expression on Logisim/Logic Works.**

**PART – A:**

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**PART – B:**

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